AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method, comprising:

determining at a requesting agent processor that Input Output (IO) traffic is to be received at a target processor cache of a target processor, wherein the target processor is different than the requesting agent processor;

receiving at a write agent, from the requesting agent processor, routing information associated with the IO traffic; ~~and~~

arranging by the write agent for information packets of the IO traffic to be transferred directly into the target processor cache in accordance with the routing information, wherein the ~~arranging is performed by~~ write agent is different than the requesting agent processor and the target processor and comprises at least one of: (i) a direct memory access controller, or (ii) a IO controller hub; and

arranging by the write agent for status information associated with the IO traffic to be transferred directly into a requesting agent cache of the requesting agent processor.

2. (previously presented) The method of claim 1, wherein the routing information is received from an IO driver executing at the requesting agent processor.

3. (previously presented) The method of claim 1, wherein the routing information includes at least one of: (i) a memory address, (ii) a target processor identifier, (iii) a direct transfer on/off indication, (iv) a cache allocation/update indication, (v) a routing policy, (vi) a

routing condition, (vii) a routing preference, (viii) coherence information, or (ix) an allocation policy.

4. (previously presented) The method of claim 1, wherein the IO traffic is associated with at least one of: (i) a network, (ii) a network interface controller, (iii) a disk drive controller, (iv) a peripheral component interconnect interface, (v) a universal serial bus interface, or (vi) a 1394 interface.

5. (original) The method of claim 1, wherein the arranging is performed in a multi-processor system that includes a plurality of potential target processor caches.

6-7. (canceled)

8. (original) The method of claim 1, further comprising:

receiving the IO traffic; and

determining whether the IO traffic should be stored in system memory or be transferred directly into the target processor cache.

9. (original) The method of claim 1, wherein the routing information indicates that one type of IO traffic should be transferred directly into the target processor cache while another type of IO traffic should be transferred directly into another target processor cache.

10. (previously presented) The method of claim 1, wherein the IO traffic is received from at least one of: (i) a network fabric, and (ii) a disk drive, a (iii) a graphics device, or (iv) a peripheral device.

11. (original) The method of claim 1, wherein the IO traffic is transferred into the target processor cache in accordance with a chipset's platform routing function.

12. (currently amended) An article, comprising:

a first computer-readable storage medium having stored thereon instructions that when executed by a machine result in the following:

determining at a requesting agent processor that Input Output (IO) traffic is to be received at a target processor cache of a target processor, wherein the target processor is different than the requesting agent processor;

a second computer-readable storage medium having stored thereon instructions that when executed by a machine result in the following:

receiving from the requesting agent processor routing information associated with the IO traffic; ~~and~~

arranging by a write agent for information packets of the IO traffic to be transferred directly into the target processor cache in accordance with the routing information, wherein the ~~arranging is performed by~~ write agent is different than the requesting agent processor and the target processor and comprises an ~~at least one of: (i) a direct memory access controller, or (ii) a~~ IO controller hub; and

arranging by the write agent for status information associated with the IO traffic to be transferred directly into a requesting agent cache of the requesting agent processor.

13. (previously presented) The article of claim 12, wherein, wherein the routing information is received from an IO driver executing at the requesting agent processor.

14. (previously presented) The article of claim 12, wherein the routing information includes at least one of: (i) a memory address, (ii) a target processor identifier, (iii) a direct transfer on/off indication, (iv) a cache allocation/update indication, (v) a routing policy, (vi) a routing condition, (vii) a routing preference, (viii) coherence information, or (ix) an allocation policy.

15-19. (canceled)

20. (currently amended) A system, comprising:

~~a network fabric;~~

a network interface controller coupled to [the] a network fabric;

a requesting agent processor having a requesting agent cache;

a target processor having a target processor cache, wherein the target processor is different than the requesting agent processor; and

a write agent comprising a direct memory access controller, including:

an input path to receive from the requesting agent processor routing information associated with ~~Input Output (IO)~~ IO traffic; and

a processing element to (i) arrange for information packets of the IO traffic to be transferred directly into [a] the target processor cache in accordance with the routing information, ~~wherein the write agent comprises at least one of: (i) a direct memory access controller, or (ii) a IO controller hub~~ and (ii) arrange for status information associated with the IO traffic to be transferred directly into the requesting agent cache.

21. (currently amended) The system of claim 20, wherein an IO driver executing at the requesting agent processor provides the routing information to the write agent.

22. (canceled)